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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,365	06/28/2001	Rumi Sheryar Gonda	S1415/7014 EJR	7514

23628 7590 01/25/2005

WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
HOM, SHICK C	

ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,365	GONDA, RUMI SHERYAR	
	Examiner	Art Unit	
	Shick C Hom	2666	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2001 and 25 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,27-30 and 33-35* is/are rejected.

7)☒ Claim(s) *22-26,31,32 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

2. Claims 4-8 and 13-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4 line 7 which recite "the tree representation" lacks clear antecedent basis because no tree representation have been previously recited in the claims and therefore the limitation is not clearly understood; further it is not clear as to whether it is reciting ---the logical representation--- of claim 3 lines 2-3.

Claims 5-8 and 13-15 are rejected under 35 U.S.C. 112, second paragraph because they depend from rejected claim 4.

3. Claims 1-3, 9-12, 19-21, and 27-30 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Application No. 09/894,420. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following:

For claims 1-3, 9-12, 19-21, and 27-30, the claims 1-8 of copending application 09/894,420 discloses a method for restoring information in a system having one or more central components each having a collection of distributed data, the distributed data being distributed among one or more distributed components., the method comprising: requesting, from the each of the one or more distributed components, the distributed data, the distributed data having connection information associated with each of the one or more distributed components; and storing the distributed data in a memory storing the collection of distributed data (see claim 1);

wherein each of the distributed components is located in at least one of a plurality of switch components, the method further comprising: defining a logical abstraction having a plurality of switch stages, each stage having at least one port; defining a physical abstraction having an associated plurality of components wherein at least one component has a physical

port; and mapping the at least one port in the logical abstraction to the physical port of the component associated with the physical abstraction (see claim 2).

further comprising: determining a logical path through the plurality of switch stages defined by the logical abstraction (see claim 3);

wherein each of the plurality of connections between each stages are represented by a logical representation, the logical representation holding state information indicating an availability of said connections, the plurality of switch stages having a plurality of connection between stages, and the method further comprises setting up a circuit between an ingress and egress port of the network system (see claim 4);

wherein the logical abstraction includes logical switch elements having logical ports identified by a logical port number, and wherein the mapping operation further comprises mapping a logical port number to the physical port of the component (see claim 5);

further comprising mapping based on a combination of chassis, slot, port, wave, and channel (see claim 6);

wherein the logical abstraction is modeled as a generic Clos switch architecture (see claim 7);

wherein the physical abstraction is modeled as a hardware-specific Clos switch architecture (see claim 8).

Claims 1 and 19 merely broaden the scope of the U.S. Application No. 09/894,420 claims 1 and 2 by eliminating the steps of requesting distributed data from the distributed components having connection information associated with the components and storing the data in a memory as recited in claim 1. Likewise, the application's claims 2-3, 9-12, 20-21, and 27-30 merely broaden the scope of U.S. Patent No. 09/894,420 claims 3-8, respectively, by eliminating the steps of requesting distributed data from the distributed components having connection information associated with the components and storing the data in a memory. It has been held that the omission of a element and its function is an obvious expedient if the remaining elements perform the same function as before. In re Karlson, 136 USPQ (CCPA). Also note Ex parte Rainu, 168 USPQ 375 (Bd. App. 1969); omission of a reference element whose function is not needed would be obvious to one skilled in the art.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple

assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 9-12, 16-21, 27-30, and 33-35 are rejected under 35 U.S.C. 102(b) as being anticipate by McMillen et al. (5,321,813).

Regarding claims 1, 18-19, and 35:

McMillen et al. disclose the method for determining a connection in a network system (see col. 22 lines 11-26 which recite wiring pattern in the connections of the network), the method comprising: defining a logical abstraction having a

plurality of switch stages, each stage having at least one port; defining a physical abstraction having an associated plurality of components wherein at least one component has a physical port (see Fig. 2 and col. 7 lines 10-27 and col. 7 line 52 to col. 8 line 13 which recite the switch nodes, each having switch stages, each stage having I/O ports whereby within the switch node, any input port can be connected to any output port, and the interconnections between switch nodes; and col. 64 lines 30-37 which recite step of defining the plurality of input and output ports including means for selectively connecting the input port to output ports); and mapping the at least one port in the logical abstraction to the physical port of the component associated with the physical abstraction as in claims 1, 19, and wherein the plurality of switch stages includes at least three switch stages as in claims 18, 35 (see Fig. 10 and col. 30 lines 3-20 which recite the routing tag, providing the logical to physical translation, to the mapping table for mapping to the output port of the switch node based on the way the network boards being cabled; further, in the preferred embodiment the switch includes node three stages); and the use of computer-readable medium as in claim 19 (see col. 5 lines 33-43 which recite using software for support of switching clearly anticipate the computer readable medium as in claim 19).

Regarding claims 2, 20:

McMillen et al. disclose the method and computer-readable medium further comprising: determining a logical path through the plurality of switch stages defined by the logical abstraction (see col. 9 lines 30-58 which recite the virtual network topology including mapping at each stage of the network and a path to every I/O port).

Regarding claims 3, 21:

McMillen et al. disclose wherein each of the plurality of connections between each stages are represented by a level of a logical representation, the logical representation holding state information indicating an availability of said connections, the plurality of switch stages having a plurality of connection between stages, and the method further comprises setting up a circuit between an ingress and egress port of the network system (see col. 38 lines 10-28 which recite the use of the connect command for selecting the output port or ports as they become available for the input port in the switch node for each stage and col. 42 line 43 to col. 43 line 7 which recite the use of the available and not-available keys to indicate ports unavailable clearly reads on the state information indicating an availability of the connections).

Regarding claims 9, 27:

McMillen et al. disclose wherein the logical abstraction includes logical switch elements having logical ports identified by a logical port number, and wherein the mapping operation further comprises mapping a logical port number to the physical port of the component (see col. 8 line 61 to col. 9 line 3 which recite referencing ports by the switch-node-port-number and col. 9 lines 30-51 which recite the mapping of the port).

Regarding claims 10, 28:

McMillen et al. disclose mapping based on a combination of chassis, slot, port, wave, and channel (see col. 10 lines 40-63 which recite the mapping table including the channel interface, port select register, and chip address register).

Regarding claims 11, 29:

McMillen et al. disclose wherein the logical abstraction is modeled as a generic Clos switch architecture (see Fig. 2 which shows a basic arrangement of a 3 stage CLOS type switch, where stage switches 1 corresponds to the intermediate stage, and the left and right stage switches 0 corresponds to the input and output stages).

Regarding claims 12, 30:

McMillen et al. disclose wherein the physical abstraction is modeled as a hardware-specific Clos switch architecture (see

Fig. 2 and col. 17 lines 29-38 which recite the hardware requirement for the switch).

Regarding claims 16, 33:

McMillen et al. disclose wherein the setting up operation includes setting up a connection in a direction from the ingress port to the egress port (see col. 38 lines 10-28 which recite establishing paths from the receiving input port to the set of selected output ports).

Regarding claims 17, 34:

McMillen et al. disclose wherein the setting up operation includes setting up a connection in a direction from the egress port to the ingress port (see col. 13 line 41 to col. 14 line 2 which recite the output ports from stage 0 switch node communicating with the input ports of a first stage 1 switch node).

Allowable Subject Matter

7. Claims 4-8 and 13-15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claims 22-26, 31-32, and 36 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
Chiussi et al. disclose multicast routing in multistage networks.
Turner discloses non-blocking multi-cast switching system.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shick C Hom whose telephone number is 571-272-3173. The examiner can normally be reached on Monday to Friday with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 5710272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH

DANG TON
PRIMARY EXAMINER